REMARKS

Claims 14-15, 17-31, 34-51, 54-64, 66-70 were pending in the application and were rejected under 35 U.S.C. 103(a) over various combinations of the following references: Okin (U.S. patent 5,361,337); Hendel (U.S. patent 5,175,732); Nemirovsky (DYNAMIC INSTRUCTION STREAM COMPUTER, Apple Computer Corporation, 1991); Hough (U.S. patent 4,604,694); and Tanenbaum (Structured Computer Organization). Some of these claims are canceled, and the remaining claims are re-written to depend from new Claims 71-80. Claims 71-80 are believed to be allowable for the following reasons.

Claim 71 is directed to handling indications that are suspended without being executed to completion. The processor of Claim 71 has two different mechanisms for handling such instructions—corresponding to "first" and "second" indications. For each first indication, the processor suspends the associated task. For each second indication, the task is not suspended and the instruction is re-executed without suspending the task (see the last two paragraphs of Claim 71).

Claim 71 is supported by the specification, page 23, lines 7-23. The first indication reads on the Suspend signal (line 8). The Suspend signal can be asserted when a resource (e.g. a FIFO) is unavailable (page 26, lines 18-21). The second indication reads on the Wait signal (page 23, line 16). In this embodiment, the Wait signal is asserted "when a condition blocking the instruction is likely to disappear" by the time the instruction is re-executed even if the instruction is re-executed immediately. Page 23, lines 24-26. For example, a Wait signal is asserted when the instruction has to wait for a dirty register to be loaded by a Load and Store Unit (LSU), or when the LSU FIFO full. See page 49. Claim 71 is not limited to the embodiments and advantages discussed herein.

Okin performs context switching on a cache miss. His system "saves the state of a first process upon a cache miss and permits the processor to begin executing a second process" instead of the first process (column 2, lines 7-13). Okin's processor does not combine two kinds of suspended instruction handling as in Claim 71.

Hendel was cited for teaching FIFOs. Hendel is no more pertinent to Claim 71 than Okin because Hendel does not teach processing of an instruction that is not to be executed to completion as in Claim 71.

Nemirovsky discloses halting an instruction stream on a load to an instruction register (page 167, first paragraph). Nemirovsky does not teach or suggest using two mechanisms to handle suspended instructions as in Claim 71.

Hough is no more pertinent than Hendel. Hough discloses test-and-set instructions (column 1, line 67 through column 2, line 4) and compare-and-swap instructions (column 3, lines 25-46), but Hough does not discuss the instruction handling if such an instruction were to be suspended without being executed to completion as in Claim 71.

Tanenbaum was cited for teaching interchangeability of hardware and software, and this teaching is no more pertinent to Claim 71 than the other four references.

Claim 72 additionally distinguishes from the five cited references by reciting that at least one first indication and at least one second indication are obtained upon accessing respective first and second unavailable resources.

The five cited references do not teach or suggest different handling of a suspended instruction depending on the type of resource as recited in Claim 72.

Claims 73-75 depend from Claim 71.

Claims 76-80 are believed to be allowable for reasons similar to the reasons given above for the respective Claims 71-75.

Any questions regarding this case can be addressed to the undersigned at the telephone number below.

EXPRESS MAIL LABEL NO.

EV 630 861 742 US

Respectfully submitted,

Michael Shenker

Michael Shenker
Patent Attorney
Reg. No. 34,250
Telephone: (408) 392-9250, ext. 212

Law Offices Of
MacPherson Kwok Chen & Heid LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110